EE/CprE/SE 491 WEEKLY REPORT 8

Date: ***Apr 3rd, 2023 – Apr 9th, 2023***

Group number: ***sddec23-08***

Project title: ***ReRAM Compute ASIC Fabrication***

Client &/Advisor: ***Henry Duwe & Cheng Wang***

Team Members/Role:

- ***Josh Thater - Mixed Signal Designer***
- ***Matt Ottersen - VLSI Designer***
- ***Aiden Petersen - Digital Designer***
- ***Regassa Dukele - VLSI Designer***

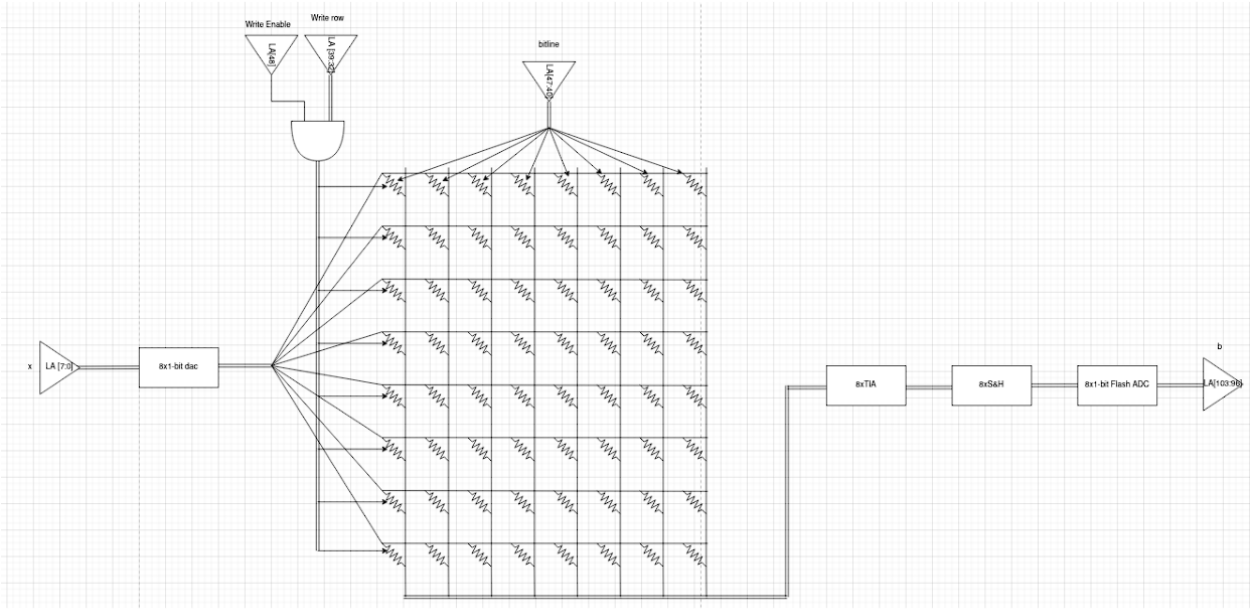
Weekly Summary

For this week, we made more progress toward getting our analog parts through the open-source process flow. We were able to simulate a sample & hold circuit, but there still is work that needs to be done on it. We also began to create a layout of the 1-bit ADC, although this is giving us some issues currently. Documentation was created on how to properly extract netlists so that LVS can be passed. Finally, we were able to extract the post-layout parasitics and simulate them. We also talked with our advisors to get a better understanding of how we will be writing to the ReRAM cells.

Past week accomplishments

- Joshua Thater
    - Created documentation on how to extract netlists to pass LVS
        - LINK: https://docs.google.com/document/d/1_9CwGs0sCGFOkvIt3-wE445qPI8kB0iz08M2xqubthE/edit?usp=sharing
    - Extracted post-layout parasitics from the layout of 1-bit DAC
    - Simulated post-layout parasitics using Xschem and Ngspice
    - Began work on attempting to simulate a ReRAM cell
- Aiden Petersen

- Top Level design
- Created top level diagram (seen below)



- Matt Ottersen
  - Created a layout for 5T op amp
  - Started working on layout for 1-bit ADC
- Regassa Dukele
  - Designed a 3-bit Analog-to-Digital Converter (ADC)
  - Working on the simulation phase to ensure correct circuit operation

Pending issues

- How to simulate the ReRAM cell (Looks like we might have to convert spice netlist to Verilog A and run simulation using Xyce?)
- How to properly create a layout of ReRAM cell using Magic
- Fully documenting the steps of how we will write to ReRAM and then compute data through ReRAM

Individual contributions

Team Member	Individual Contributions	Weekly Hours	Total Hours
Joshua Thater	Wrote documentation on how to pass LVS and simulated post-layout parasitics of 1-bit DAC	7	52
Aiden Petersen	Created top level diagram for whole project	4	45

Matt Ottersen	Created layout for Op amp and started working on layout for ADC	6	44
Regassa Dukele	Designed a 3-bit ADC and currently working on simulation and layout stages	6	43.5

Plans for the upcoming week

- Joshua Thater
    - Attempt to simulate ReRAM cell either through the interface of Ngspice or through Xyce
    - Help other members get through the process flow of their analog components
    - If time allows, begin work on transimpedance amplifier
- Aiden Petersen
    - Further refine top level diagram
    - Read into how ReRAM on Sky130 works.
- Matt Ottersen
    - Get Op Amp to Pass LVS
    - Finish 1 bit ADC layout and pass LVS
    - Simulate post layout parasitics of both
- Regassa Dukele
    - Verify design simulation and make the layout
    - Simulate design and ensure correct operation